REMARKS

Claims 1-11, 13-15, 18, 20-28, 30-35, 37 and 38 are currently pending in the subject application, and are presently under consideration. Claims 1-11, 13-15, 18, 20-28, 30-35, 37 and 38 are rejected. Claim 30 has been amended. Favorable reconsideration of the application is requested in view of the amendments and comments herein.

I. Double Patenting Rejection

Claims 1, 2, 13, 14, 15, 25, 26, 30, 37 and 38 are rejected on the ground of non-statutory obviousness-type double patenting rejection as being unpatentable over U.S. Patent No. 7,046,057 to Culler ("Culler") in view of U.S. Patent Application No. 2003/0052662 to Bi et al. ("Bi"). A terminal disclaimer is submitted herewith to overcome this rejection. Accordingly, withdrawal of this rejection is respectfully requested.

II. Rejection of Claims 30-35 and 37 under 35 U.S.C. 102(e)

Claims 30-35 and 37 have been rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,701,445 to Majos ("Majos"). Withdrawal of this rejection is respectfully requested for at least the following reasons.

Claim 30 has been amended to make explicit that which was believed to be implicit. Specifically, claim 30 has been amended to recite determining a frequency value for a signal that represents a frequency of the signal. In rejecting claim 30, the Office Action contends that signals H+ and H- disclosed in Majos read on frequency values. Applicant's representative respectfully submits that in amended claim 30, the frequency value determined represents a frequency of a signal. Majos fails to disclose (or even suggest) that either H+ or H- represents a frequency of a signal. Instead, in Majos, H+ and H- represent a comparison between two frequencies of signals at 1E (e.g., Din) and 1H (See Majos, Col. 6, Line 60-Col. 7, Line 20). Accordingly, Majos does not disclose determining a frequency value for a signal that represents a frequency of the signal based on (i) output samples received at a detector that correspond to time instances of the signal residing within a single period of the signal, and (ii) predetermined and spaced apart time intervals, as recited in amended claim 30. Thus, Majos does not anticipate amended claim 30, since Majos does not disclose determining a frequency value as recited in

amended claim 30. Therefore, amended claim 30, as well as claims 31-35 and 37 depending therefrom are patentable.

III. Rejection of Claims 1, 2, 9, 11, 13, 14, 25, 26-28 under 35 U.S.C. 103(a)

Claims 1, 2, 9, 11, 13, 14, 25, 26-28 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Majos. Withdrawal of this rejection is respectfully requested for at least the following reasons.

In rejecting claim 1, the Office Action contends that an upcounter-downcounter 4 (hereinafter "up/down counter 4") disclosed in Majos corresponds to a comparator recited in claim 1 (See Office Action, Page 6). Applicant's representative respectfully disagrees. The up/down counter 4 disclosed in Majos adjusts a control voltage (via a digital-to-analog converter (DAC) 5) of a voltage controlled oscillator (VCO; See Majos, Col. 8, Lines 16-35). In distinction, the comparator recited in claim 1 provides a comparator signal based on a comparison of a value of a frequency for an input signal and a value of a desired frequency (from a detector). Thus, the up/down counter 4 disclosed in Majos performs a substantially different function from the comparator recited in claim 1. This difference stems from the inclusion of a detector in claim 1 that provides a value that represents the determined frequency of the input signal, whereas Majos employs a frequency comparator 3 to provide two one-bit signals, H- and H+ and a sampling signal HE as inputs to the up/down counter 4 (See Majos, FIG. 1).

For instance, the inputs to the up/down counter 4 are two one-bit signals, H- and H+ and a sampling signal HE (See Majos, FIG. 1). None of these inputs (H-, H+ and HE) to the up/down counter 4 disclosed in Majos corresponds to the values of the frequency of the input signal and desired frequency, as recited in claim 1. That is, in contrast to the values of frequency recited in claim 1, none of the inputs (H-, H+ and HE) to the up/down counter 4 disclosed in Majos would allow ascertainment of the frequency of either input signal or the desired frequency. Instead, the input (H-, H+ and HE) to the up/down counter 4 disclosed in Majos provide only a relative indication of a comparison of frequencies.

Moreover, the Office Action contends (at page 7, second and third paragraphs) that in one embodiment of Majos, (illustrated in FIG. 5), a frequency of an input data signal (Hr) is known, and that in such an embodiment, when both H- and H+ are logical '0', thus indicating that signals

1H and 1E have equal frequencies, that H- and H+ correspond to the values of frequency recited in claim 1. Applicant's representative respectfully disagrees. As stated above, the comparator recited in claim 1 provides a comparison signal based on a comparison of a value of a frequency of an input signal and a comparison of a value of a desired frequency. Applicant's representative respectfully submits that regardless of whether certain information (which is not input into the up/down counter 4) could be employed to ascertain the frequency of signal 1H when signal 1H has a frequency equal to signal at 1E is not material. There is no teaching or suggestion in Majos and no other evidence of record to support a position that one of ordinary skill in the art would deem the results predictable, as such a proposition would require adding circuitry, complexity and cost in to the system of Majos in order do something unnecessary for the intended purpose of Majos. In claim 1, the frequency values (already determined by the detector) are provided as inputs to the comparator. Thus, there is no teaching or suggestion in Majos that the up/down counter 4 provides a comparator signal based on a comparison of a value of a frequency for an input signal and a value of a desired frequency, as does the comparator recited in claim 1. Therefore, Majos does not teach or suggest the system of claim 1 since Majos fails to teach or suggest any structure or process that corresponds to the comparator recited in claim 1. Consequently claim 1, as well as claims 2, 9, 11, 13 and 14 depending therefrom, is patentable.

Claim 25 is similar to claim 1. Specifically, claim 25 recites means for comparing a frequency value relative to a desired frequency value. For reasons similar to those discussed above with respect to claim 1, Majos fails to teach or suggest the means for comparing recited in claim 25. Therefore, Majos fails to teach or suggest the system of claim 25. Accordingly, Majos fails to make claim 25 obvious, since Majos fails to teach or suggest the system recited in claim 25. Thus, claim 25, as well as claims 26-28 depending therefrom, is patentable.

For at least the reasons stated above, claims 1, 2, 9, 11, 13, 14, 25, 26-28 are patentable. Accordingly, withdrawal of this rejection is respectfully requested.

IV. Rejection of Claims 3-8, 10, 15, 18, 20-24 and 38 under 35 U.S.C. 103(a)

Claims 3-8, 10, 15, 18, 20-24 and 38 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Majos, in view of U.S. Patent No. 6,326,826 to Lee, et al. ("Lee"). Withdrawal of this rejection is respectfully requested for at least the following reasons.

Claims 3-8 and 10 depend from claim 1. The addition of Lee does not make up for the aforementioned deficiencies of Majos with respect to claim 1. In rejecting claims 3-8 and 10, the Office Action relies on Lee solely for Lee's disclosure of detection cells 22' (See Office Action, Pages 8-9). Accordingly, Majos taken in view of Lee fails to make claims 3-8 and 10 obvious, and claims 3-8 and 10 are patentable. Thus, the rejection of claims 3-8 and 10 should be withdrawn.

Regarding claim 15, the Office Action contends that the output of an XOR gate 10 and the output of a delay line 12 disclosed in Majos corresponds to a plurality of delay elements recited in claim 15. Specifically, the Office Action contends that the output of XOR gate 10 goes to delay 12 and a "0" delay path 10 to 14, which can be thought of as a delay element with "0" delay (See Office Action, Page 12). Applicant's representative respectfully disagrees. There is no teaching or suggestion in Majos to support the argument that the output of XOR gate 10 provided to flip flops 14 and 15 is delayed by "0" and therefore reads on a delay element. Applicant's representative respectfully submits that even under the broadest reasonable interpretation of "delay element," a connection that does not provide any known amount of delay to a signal (e.g., the connection between XOR gate 10 and flip flops 14 and 15) cannot correspond to a delay element, as recited in claim 15.

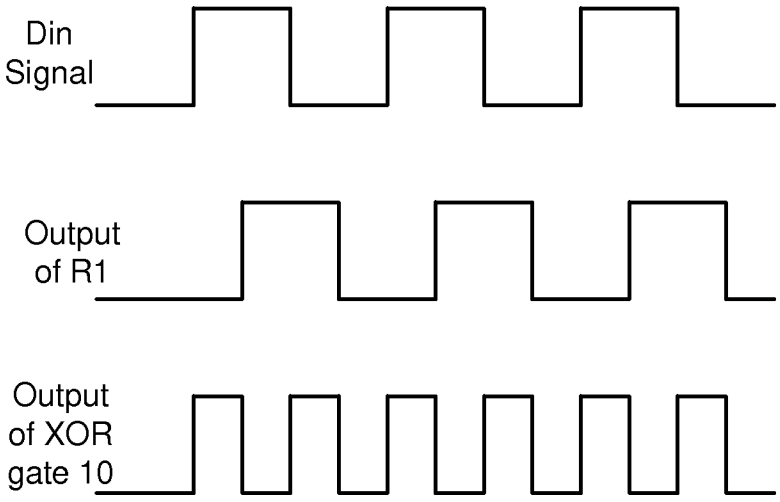
Moreover, it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. *In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q. 2d 1780 (Fed. Cir. 1992). Applicant's representative respectfully submits that the Office Action is impermissibly using claim 15 as the aforementioned "template" in an attempt to make claim 15 obvious. Specifically, the only motivation to even attempt to consider the connection between XOR gate 10 and flip flops 14 and 15 a delay element is claim 15 itself.

Furthermore, the Office Action argues that in an alternative argument, one of ordinary skill could put on more delay elements in the path of 10 to 14 for a different design, and such a modification is possible within the scope of Majos and can provide better sampling of H (See Office Action, Page 13, lines 1-4). Applicant's representative respectfully disagrees. The Office Action fails to explain how adding additional delay elements between XOR gate 10 and flip flop 14 disclosed in Majos would provide better sampling of signal H. Thus, the Office Action fails

to provide the necessary articulated reasoning with some rational underpinning to support the legal conclusion of obviousness (35 U.S.C. §103) consistent with the mandates of KSR. *KSR International Co. v. Teleflex Inc. (KSR)*, 550 U.S. ___, 82 USPQ2d 1385 (2007). Applicant's representative respectfully submits that such an addition of a delay element would be completely superfluous, and that the only reason to do so would be an attempt to make claim 15 obvious (once again impermissibly using claim 15 as a "template."). Thus, since the Office Action has impermissibly used claim 15 as a "template", Applicant's representative respectfully submits that the differences between claim 15 and the art of record demonstrates that claim 15 is not obviousness. Accordingly, claim 15, as well as claims 18, 20-24 and 38 depending therefrom, is patentable.

Additionally, Majos taken in view of Lee does not teach or suggest that an input signal comprises a sample signal, and that the input signal is delayed by a plurality of delay elements to provide respective delayed clock signals, as recited in claim 18. In rejecting claim 18, the Office Action contends that Lee discloses delaying an input signal (REF_CK), and thus makes claim 18 obvious (See Office Action, Page 13). Applicant's representative respectfully submits that the Office Action is offering interpretations of Majos and Lee inconsistent with the rejection of claim 15 (from which claim 18 depends) in an effort to make claim 18 obvious.

Specifically, as stated above, in rejecting claim 15, the Office Action contended that the output of XOR gate 10 corresponds to a sample signal (See Office Action, Page 12). In claim 15 (from which claim 18 depends), a sample signal is delayed. As shown in FIG. 2 of Majos, the output of XOR gate 10 could not be replaced by an input signal (e.g., signal 1H) since in Majos, the system is designed such that the output of XOR gate 10 has a different frequency than the input signal at 1E (e.g., Din). In Majos, the output of the XOR gate 10 is a waveform having a frequency and duty cycle that depends on the frequency of the data signal Din and on the amount of delay provided by R1. To illustrate this concept, Applicant's representative respectfully submits the following diagram:



The output of the XOR gate 10 is clearly not a delayed version of the input signal at 1E (e.g., Din). Thus, any suggestion by the Office Action to replace the output signal of XOR gate 10 with the input signal would be inconsistent with the rejection of claim 15, from which claim 18 depends, since the output of the XOR gate 10 is not merely a delayed version of another signal.

Moreover, The U.S. Court of Appeals for the Federal Circuit has held that references teach away from their combination if the references taken in combination would produce a seemingly inoperable device. *McGinley v. Franklin Sports Inc.*, 262 F.3d 1339, 1354, 60 U.S.P.Q.2D 1001, 1010 (Fed. Cir. 2001). Replacing the output of the XOR gate 10 with an input signal and delay elements (as suggested by the Office Action in the rejection of claim 18) would require eliminating the XOR gate 10. As is known, delaying an input signal, such as the signal at 1E (e.g., by adding delays 18 disclosed in Lee) would not change the frequency of the input signal at 1E, which is required for proper operation of the system disclosed in Majos (See e.g., Majos, Col. 5, Lines 18-14). Thus, the purported combination of Majos and Lee suggested in the rejection of claim 18 would result in a seemingly inoperable device. Therefore, Applicant's representative respectfully submits that there is no motivation to combine and modify the teachings of Majos and Lee in the manner suggested by the Office Action. Consequently, Majos taken in view of Lee does not make the system of claim 18 obvious, since Majos taken in view of Lee does not teach or suggest an input signal comprises a sample signal, and that the input signal is delayed by a plurality of delay elements to provide respective delayed clock signals, as recited in claim 18.

Furthermore, claim 38 recites that the frequency value is expressed in units of an inverse of a period of an input signal. In rejecting claim 38, the Office Action admits that H+ and H- are not expressed in units of an inverse period, but contends in a second embodiment (illustrated in FIG. 5) of Majos, H+H-=00 implies that signals at 1E (e.g., Hr) and 1H have the same frequency, and it is possible for one of ordinary skill to express the frequency in units of Hertz (Hz; See Office Action, Page 14). In such a situation, the Office Action must assume that the frequency of a clock signal (e.g., Hr) is known. Applicant's representative respectfully submits that the Office Action's reasoning clearly illustrates a deficiency of the system taught in Majos, which highlights differences between the system recited in claim 38 and the system of Majos that weigh in favor of a conclusion of nonobviousness. In claim 38, a frequency value is expressed in units of an inverse of a period of an input signal. There is no requirement in claim 38 (either expressed or implied) that the frequency value (e.g., the inverse of a period) of the input signal is known. Therefore, Majos does not make claim 38 obvious since Majos does not teach or suggest that the frequency of H+ or H- is expressed in units of an inverse of a period of an input signal, in contrast to the frequency value recited in claim 38.

V. CONCLUSION

In view of the foregoing remarks, Applicant respectfully submits that the present application is in condition for allowance. Applicant respectfully requests reconsideration of this application and that the application be passed to issue.

Should the Examiner have any questions concerning this paper, the Examiner is invited and encouraged to contact Applicant's undersigned attorney at (216) 621-2234, Ext. 106.

No additional fees should be due for this response. In the event any fees are due in connection with the filing of this document, the Commissioner is authorized to charge those fees to Deposit Account No. 08-2025.

I hereby certify that this correspondence is being transmitted to the U.S. Patent and Trademark Office via electronic filing on April 15, 2008.

Respectfully submitted,

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